33. (New) The memory device of claim 31, wherein said suspend signal represents a byte write suspend command.

34. (New) The memory device of claim 31, wherein said control circuit is configured to receive a status request signal and said register is configured to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

35. (New) The memory device of claim 35, further comprising:

at least one data input/output coupled to said control circuit, wherein the at least one data input/output is configured to receive said status request signal from a processor and to provide said status signal to said processor.

36. (New) The memory device of claim 31, further comprising:

a status output coupled to said register, wherein said status output is configured to provide a second status signal when said status output is polled, and wherein said second status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

37. (New) The memory device of claim 31, wherein said status request signal is a read status register command.